a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer, wherein said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer, and said third semiconductor layer is in direct contact with said second semiconductor layer and so that said fourth semiconductor layer does not contact with said second semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on portions of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said portions through said insulating film so that said portions form channel regions of said insulated gate semiconductor device, and said fourth semiconductor layer is the only semiconductor layer where said channel regions are formed.